Application number 09/835,021 PATENT
Amendment dated June 3, 2003
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This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-2 (Cancelled)

Claim 3. (Currently amended) A method of buffering an input signal comprising:

receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

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generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein a capacitance is between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit, ~~and~~

wherein the input signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal, and

wherein the first current and the second current are generated by transistors that are biased to have gate-source voltages approximately equal to their threshold voltages.

Claim 4. (Previously amended) The method of claim 3 wherein the first current and the second current are generated by NMOS devices.

Claim 5. (Original) The method of claim 4 wherein the third current and the fourth current are generated by PMOS devices.

Claim 6. (Currently amended) A method of buffering an input signal comprising:

receiving the input signal, wherein the input signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the input signal when the input signal has the first polarity, and approximately equal to zero when the input signal has the second polarity;

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generating a second current, wherein the second current is proportional to the input signal when the input signal has the second polarity, and approximately equal to zero when the input signal has the first polarity;

generating a third current proportional to the first current;

generating a fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein a capacitance is between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit, ~~and~~

wherein the first current is geometrically proportional to the input signal when the input signal has the first polarity, and the second current is geometrically proportional to the input signal when the input signal has the second polarity, and

wherein the first current and the second current are generated by transistors that are biased to have gate-source voltages approximately equal to their threshold voltages.

Claims 7-16. (Cancelled)

Claim 17. (Currently amended) A circuit for buffering RF signals comprising:

a first device coupled between a first output node and a first supply node, having a control electrode coupled to a first input node;

a second device coupled between a second output node and the first supply node, having a control electrode coupled to a second input node;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node;

a fifth device coupled between the first device and the first output node;

a sixth device coupled between the second device and the second output node;

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a seventh device coupled between a current source and the first supply node, having a control electrode coupled to the first input node and the second input node; and

an inductor coupled between the first output node and the second output node.

Claim 18. (Previously amended) The circuit of claim 17 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

Claim 19. (Original) An integrated circuit, wherein the integrated circuit comprises the circuit of claim 18.

Claim 20. (Original) A transceiver comprising the circuit of claim 18.

Claim 21. (Original) An computing device comprising:

a memory;

a central processing unit coupled to the memory; and

the transceiver of claim 20 coupled to the central processing unit.

Claim 22. (Cancelled)

Claim 23. (Currently amended) A method of buffering an RF signal comprising:

receiving the RF signal, wherein the RF signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the RF signal when the RF signal has the first polarity, and approximately equal to zero when the RF signal has the second polarity;

generating a second current, wherein the second current is proportional to the RF signal when the RF signal has the second polarity, and approximately equal to zero when the RF signal has the first polarity;

using the first current to generate a third current, the third current proportional to the first current;

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using the second current to generate a fourth current, the fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein a capacitance is coupled between the first terminal of the inductor and the second terminal of the inductor, and the inductor and capacitance form a tank circuit, and

wherein the first current and the second current are generated by transistors that are biased to have gate-source voltages approximately equal to their threshold voltages.

Claim 24. (Previously amended) The method of claim 23 wherein the RF signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency of a second frequency, and the first frequency and second frequency are approximately equal.

Claim 25. (Previously amended) A method of buffering an RF signal comprising:

receiving the RF signal, wherein the RF signal alternates between a first polarity and a second polarity;

generating a first current, wherein the first current is proportional to the RF signal when the RF signal has the first polarity, and approximately equal to zero when the RF signal has the second polarity;

generating a second current, wherein the second current is proportional to the RF signal when the RF signal has the second polarity, and approximately equal to zero when the RF signal has the first polarity;

using the first current to generate a third current, the third current proportional to the first current;

using the second current to generate a fourth current, the fourth current proportional to the second current;

applying the first and fourth currents to a first terminal of an inductor; and

applying the second and third currents to a second terminal of the inductor,

wherein the first current is geometrically proportional to the RF signal when the RF signal has the first polarity, and the second current is geometrically proportional to the RF signal when the RF signal has the second polarity.

Claim 26. (Cancelled)

Claim 27. (Currently amended) An RF amplifier comprising:

a first device coupled between a first output node and a first supply node, having a control electrode configured to receive an RF signal, and further configured to operate near cutoff ~~in the absence of the RF signal~~ when the RF signal has an amplitude of zero volts;

a second device coupled between a second output node and the first supply node, having a control electrode configured to receive a complement of the RF signal, and further configured to operate near cutoff ~~in the absence of the complement of the RF signal~~ when the RF signal has an amplitude of zero volts;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node;

a fifth device coupled between the first device and the first output node;

a sixth device coupled between the second device and the second output node; and

an inductor coupled between the first output node and the second output node.

Claim 28. (Previously added) The circuit of claim 27 wherein the first device and the second device are NMOS devices, and the third device and fourth device are PMOS devices.

Claim 29. (Previously added) An integrated circuit, wherein the integrated circuit comprises the circuit of claim 28.

Claim 30. (Previously added) A transceiver comprising the circuit of claim 28.

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Claim 31. (New) The circuit of claim 17 wherein the seventh device receives a current from the current source and biases the first device and the second device.

Claim 32. (New) The circuit of claim 31 wherein the first device and the second device are biased to have gate-to-source voltages approximately equal to their threshold voltages.

Claim 33. (New) The method of claim 25 wherein a first terminal of a capacitor is coupled to the first terminal of the inductor.

Claim 34. (New) The method of claim 33 wherein a second terminal of the capacitor is coupled to the second terminal of the inductor and the capacitor and inductor form a tank circuit.

Claim 35. (New) The method of claim 34 wherein the RF signal alternates between the first polarity and the second polarity at a first frequency, the tank circuit has a resonant frequency at a second frequency, and the first frequency and second frequency are approximately equal.

Claim 36. (New) The method of claim 33 wherein the first current and the second current are generated by transistors that are biased to have gate-source voltages approximately equal to their threshold voltages.

Claim 37. (New) A circuit for amplifying RF signals comprising:

a first device coupled between a first output node and a first supply node, having a control electrode coupled to a first input node;

a second device coupled between a second output node and the first supply node, having a control electrode coupled to a second input node;

a third device coupled between a second supply node and the first output node, having a control electrode coupled to the second output node;

a fourth device coupled between the second supply node and the second output node, having a control electrode coupled to the first output node;

a fifth device coupled between a current source and the first supply node, having a control electrode coupled to the first input node and the second input node; and

an inductor coupled between the first output node and the second output node.

Claim 38. (New) The circuit of claim 37 wherein the first device, the second device, and the fifth device are NMOS devices, and the third device and fourth device are PMOS devices.

Claim 39. (New) The circuit of claim 37 wherein the seventh device receives a current from the current source and biases the first device and the second device.

Claim 40. (New) The circuit of claim 39 wherein the first device and the second device are biased to have gate-to-source voltages approximately equal to their threshold voltages.